HIGH-FANIN STATIC MULTIPLEXER

Brian J. Campbell

ABSTRACT OF THE DISCLOSURE

[023] An improved high-fanin multiplexer that is highly-scalable, fast and area-efficient. In one embodiment of the present invention, multiple logic "legs" are attached to a common output line. Each leg comprises one pMOS pull-up transistor and one nMOS pull-down transistor. The gate of the pMOS transistor in each leg is connected to the output of an And-Or-Invert (AOI) gate whose inputs are connected to a plurality of select lines and a plurality of data lines. The gate of the nMOS transistor in each leg is connected to the output of an Or-And-Invert (OAI) gate whose inputs are connected to a plurality of select lines (the logical complements of the select lines for the AOI), and a plurality of data input lines. The high-fanin multiplexer of the present invention offers numerous advantages over the prior art. In particular, the high-fanin multiplexer of the present invention has very small self-loading allowing a large number of inputs while also maintaining a high fan out speed. In addition, the small input capacitive load allows the driving gates to be small, thereby conversing surface area within an integrated circuit.